REMARKS/ARGUMENTS

Prior to this Amendment, claims 1-30 were pending in this application.

Claim 1 is amended to clarify operation of the multiplexor in response to an owner signal which is generated based on a state value associated with a peripheral-share register of a peripheral unit.

Independent claim 9 is amended to stress the location of a stored peripheral ownership state value, i.e., in a register associated with each of the peripheral units.

Independent claim 13 is amended to include the limitations of claim 17, which is canceled.

Claims 20-24 are canceled.

Claims 25, 26, 27, and 29 are amended to correct minor errors that had created antecedent issues.

No new matter is added by the claim amendments. Claims 1-16, 18, 19, and 25-30 remain in the application for consideration by the Examiner.

Rejections under 35 U.S.C. 112

Claims 27 and 29 were rejected under 35 U.S.C. 112, second paragraph as being indefinite. Claims 25, 26, 27 and 29 have been amended to address antecedent issues with "the plurality of processors" and "the controller of claim 28."

Double Patenting Rejection

The Office Action rejected claims 1-2, 4-12, and 20-29 under the judicially created doctrine of obviousness-type double patenting. The Office Action indicated that timely filing of a terminal disclaimer could be used to overcome this rejection. In response, a terminal disclaimer is provided that complies with 37 CFR 1.321(c) to address this rejection.

Rejection under 35 U.S.C. 103 of Claims 1-2, 5, 7-8, and 25-28

In the Office Action, claims 1-2, 5, 7-8, and 25-28 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,408,671 ("Tanaka") in view of U.S. Pat. No. 5,408,627 ("Stirk") and further in view of U.S. Pat. No. 5,889,947 ("Starke"). This rejection is respectfully traversed based on the following remarks.

Claim 1 calls for an embedded computing system comprising a plurality of processors and a bus coupling to a plurality of peripheral units. This multiprocessing architecture within a disk drive controller is not shown or suggested by the relied on references. Tanaka discloses a multiprocessor system having multiple processors coupled to memory registers not peripherals. Tanaka, however, does not show or suggest using the claimed multiprocessor architecture in an embedded computing system. For at least this reason, claim 1 is believed allowable over Tanaka.

Claim 1 further calls for a multiplexor for selectably coupling each of the plurality of processors to the bus in response to an owner signal. The Office Action states that Tanaka fails to teach such a multiplexor and cites Stirk at data MUX 46, address MUX 50, and associated circuits for teaching the multiplexor of claim 1. While Stirk shows the use of multiplexors, it fails to show coupling outputs of such processors to shared peripherals "in response to an owner signal" but instead apparently operates the data write MUX 46 and address MUX 50, at least in part, with an arbitration state machine 52, which is different than the use of an owner signal as called for in claim 1.

Further, claim 1 calls for a set of peripheral-share registers including an "entry associated with each of the plurality of peripheral units holding a state value indicating which of the plurality of processors currently owns the associated peripheral unit, wherein the owner signal is based on one of the state values." Stirk fails to teach that its multiplexors are operated based on a owner signal and certainly, does not teach that the owner signal is based on the one of the state values in an entry of a state register associated with a peripheral unit. Tanaka does not overcome this deficiency with its "shared register control

portion." The Office Action cites Starke for teaching an embedded system, but Starke fails to teach the control of a multiprocessor with an owner control signal or basing the owner signal on a state value indicating ownership of a peripheral unit. Because the combination of the three references fails to teach or suggest each element of claim 1, the rejection is improper and should be withdrawn.

Claims 2, 5, 7, and 8 depend from claim 1 and are believed allowable as depending from an allowable base claim. Additionally, claim 5 calls for the set of peripheral share registers to include release registers corresponding to the processors and having an entry associated with each one of the peripheral units to hold a value indicating whether the processor is releasing ownership. The Office Action cites Tanaka for teaching this limitation with elements M1 through M4. However, these are storage areas that are described at col. 3, lines 65-68 as corresponding to the processors. There is no teaching that in the storage area an entry holding a value is stored that indicates whether one of the processor is releasing one or more peripheral devices or units. Claim 8 calls for one of the processors to be able to dynamically alter the state value used to generate the owner signal. Tanaka is cited at col. 4, lines 33-66 for teaching this element but at this citation, Tanaka is merely discussing accessing shared registers R1-R4 with processors P1-P4 and is not teaching a processor altering state values that control which of the processors can access peripheral units. For these additional reasons, claims 5 and 8 are believed allowable over the combined teaching of the references.

As with claim 1, independent claim 25 includes a multiplexor that selectively couples the processors. This is done "in response to an owner signal." As discussed with reference to claim 1, the Stirk reference shows multiplexors that respond to an arbitration machine but do not respond to "an owner signal." Further, claim 25 calls for the processors, the peripheral units, and the multiplexor to comprise a single integrated circuit. Starke shows a single IC but fails to teach processors, peripheral units, and a multiplexor as described in claim 25 within an integrated circuit and neither Tanaka nor Stirk provide any motivation to modify their designs based on the teaching of Starke. For these reasons, claim 25 is believed allowable over the cited references.

Claims 26-28 depend from claim 25 and are believed allowable for the reasons provided for allowing claim 25. Additionally, claim 26 calls for the integrated circuit to include peripheral registers with an entry for each peripheral unit holding a state value indicating the owner of the unit. As discussed with reference to claim 1, the references fail to teach peripheral registers, and particularly, such registers that hold an ownership-indicating state value. Yet further, such registers are not shown in an IC including a multiplexor, processors, and peripheral units. Claim 27 is believed allowable for the reasons provided for allowing claim 10. Claim 28 further defines the multiplexor and indicates how the portions are operated according to the state of the owner signal, which is not shown by the references. For these additional reasons, the rejection of claims 26-28 based on Tanaka, Stirk, and Starke is improper, and Applicants respectfully request that this rejection be withdrawn.

Rejection under 35 U.S.C. 103 of Claims 3 and 30

Claims 3 and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Starke further in view of U.S. Pat. No. 6,480,952 ("Gorishek"). This rejection is respectfully traversed based on the following remarks.

Claims 3 and 30 depend from claims 1 and 25, respectively, and are believed allowable as depending from an allowable base claim. Particularly, Gorishek fails to overcome the deficiencies noted for Tanaka, Stirk, and Starke with reference to claims 1 and 25, e.g., Gorishek fails to teach a multiplexor that couples processors to a peripheral bus based on an owner signal.

Rejection under 35 U.S.C. 103 of Claims 4 and 29

In the Office Action, claims 4 and 29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Stark further in view of U.S. Pat. No. 5,317,749 ("Dahlen"). This rejection is respectfully traversed based on the following remarks.

Claims 4 and 29 depend from claims 1 and 25, respectively, and are believed allowable as depending from an allowable base claim. Particularly, Dahlen fails to overcome the deficiencies noted for Tanaka, Stirk, and Starke

with reference to claims 1 and 25. Dahlen fails to teach a multiplexor that couples processors to a peripheral bus based on an owner signal.

Rejection under 35 U.S.C. 103 of Claim 6

In the Office Action, claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Stark further in view of U.S. Pat. No. 5,678,026 ("Vartti"). This rejection is respectfully traversed based on the following remarks.

Claim 6 depends from claim 1 and is believed allowable as depending from an allowable base claim. Further, Vartti fails to overcome the deficiencies noted for Tanaka, Stirk, and Starke with reference to claim 1.

Rejection under 35 U.S.C. 103 of Claims 9-12

In the Office Action, claims 9-12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dahlen in view of U.S. Pat. No. 5,317,749 ("Lehman"). This rejection is respectfully traversed based on the following remarks.

Claim 9 is directed to a method with limitations similar, but in different form, to claim 1 (without calling for the coupling to be performed based on an owner signal). Further, claim 9 calls for "dynamically altering the state values to create dynamic ownership associations between a peripheral and the plurality of processors." Dahlen when combined with Lehman fails to teach or suggest each limitation of claim 9, and hence, this rejection should be withdrawn.

Particularly, Dahlen discloses a multiprocessor system comprising multiple processors that share physical devices such as printers and direct attached storage devices (DASD). The Office Action cites Dahlen at col. 7, lines 1-7 for teaching selectively coupling but at this citation Dahlen discusses altering a latch-control word to indicate a processor has control of a resource. Dahlen does not teach selective coupling based on the value of the word let alone based on a state value associated with a peripheral unit. Lehman fails to overcome this deficiency and is only cited for the "controller" aspect of claim 9. Further, the state value is stored in a register associated with each of the peripheral units, and Dahlen fails to teach their latch-control words are stored in registers

associated with resources or peripheral units. For these reasons, claim 9 and claims 11-12 which depend from claim 9 are not taught or suggested by the combined teachings of Dahlen and Lehman.

Rejection under 35 U.S.C. 103 of Claims 13-19

In the Office Action, claims 13-19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Starke further in view of Lehman. This rejection is respectfully traversed based on the following remarks.

Claim 13 is directed to a multiprocessor controller with limitations similar to claim 1, and hence, claim 13 is believed allowable over Tanaka, Stirk, and Starke for the reasons provided for allowing claim 1. Lehman does not overcome the deficiencies of these three references. Claim 14-16, 18, and 19 depend from claim 13 and are believed allowable as depending from an allowable base claim.

Rejection under 35 U.S.C. 103 of Claims 20-21 and 23

In the Office Action, claims 20-21 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk. Claims 20-21 and 23 are canceled by this Amendment.

Rejection under 35 U.S.C. 103 of Claim 22

In the Office Action, claim 22 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Stark. Claim 22 is canceled by this Amendment.

Rejection under 35 U.S.C. 103 of Claim 24

In the Office Action, claim 24 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Stark further in view of U.S. Pat. No. 6,502,167 ("Tanaka A"). Claim 24 is canceled by this Amendment.

Conclusions

The references made of record but not relied upon in the Office Action have been considered but are believed no more relevant than those cited and relied upon by the Examiner. Hence, the pending claims are believed allowable over these additional references considered alone or in any combination.

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

A check is provided for the fees due with this Amendment. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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